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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,815	03/26/2004	Yoshihiro Hori	65933-083	7932
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EXAMINER				
LAFORGLA, CHRISTIAN A				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/809,815

Applicant(s)

HORI ET AL.

Examiner

Christian LaForgia

Art Unit

2439

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 April 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 3-16 and 18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3-16 and 18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB-08)
Paper No(s)/Mail Date 6/15/09
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. The amendment of 28 April 2009 has been noted and made of record.
2. Claims 1, 3-16, and 18 have been presented for examination.
3. Claims 2 and 17 have been cancelled as per applicant's amendment.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-16 and 18 have been considered but are moot in view of the new grounds of rejection set forth below.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 15 June 2009 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1 and 3-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicant's have amended independent claims 1 and 7 to as follows: "the cryptographic processing unit receives a plurality of subprocesses respectively belonging to two or more different cryptographic input and output processes via the bus and in a time-division

manner[] . . ." (emphasis added). After reviewing the specification, the examiner was unable to find any support that data is transmitted in a time division manner. In order to overcome the rejection, the applicant is required to point specifically to the section of the specification that supports this newly added limitation.

Claim Rejections - 35 USC § 103

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims 1, 3-5, 7, 8, 10-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 7,158,637 to Ohta et al., hereinafter Ohta, in view of U.S. Patent No. 6,275,909 B1 to Arimilli et al., hereinafter Arimilli, and in further view of U.S. Patent No. 4,238,854 to Ehrsam et al., hereinafter Ehrsam.

10. Regarding Claims 1 and 7, Ohta discloses a storage devices comprising:
a storage medium for retaining data (column 7 lines 43-53); and
a cryptographic processing unit (figure 3 Encryption and Authentication Processing Control Unit) which receives, from a host device, and executes a command corresponding to each of the plurality of sequenced subprocesses produced by dividing each of a series of cryptographic input/output processes for encrypting data to be secured and inputting/outputting the data between the storage medium and the host device, (column 6 lines 1-20, and description of figure 3 particularly in column 6 lines 39-58), wherein

a bus for receiving the command from the host device (Figures 12 [element 302], 14 [402], it is also well-known that computing systems comprise various buses to connect various devices and peripherals), wherein

the cryptographic processing unit simultaneously processes subprocesses respectively belonging to two or more different cryptographic input and output processes via the bus and in a time-division manner, to identifying information attached to the command, identifies to which cryptographic input/output process the command belongs (column 2 lines 7-11).

11. Ohta does not teach wherein the bus being deallocated for another command when the command is issued and wherein the cryptographic processing unit manages the sequence of commands executed in each cryptographic input/output processing and rejects the execution of an incorrectly sequenced command when the cryptographic processing unit receives the incorrectly sequenced command.

12. Arimilli teaches a system controller that manages a plurality of electrical devices, wherein a bus is deallocated based on a received command (column 2, line 64 to column 3, line 13).

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the bus to be deallocated when a command was issued, since Arimilli states at column 3, lines 9-13 that it would support upgrades of coherency state information, thereby providing for a more stable system.

14. Ehrtam discloses wherein the cryptographic processing unit manages the sequence of commands executed in each cryptographic input/output processing (column 14, lines 6-58, column 53, lines 11-59, column 58, lines 31-67) and issuing a procedural error when an incorrect sequence of commands is received (column 36, line 61 to column 37, line 13, column 80, line 3-67).

15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to manage the sequence of commands executed in each cryptographic input/output processing and reject the execution of an incorrectly sequenced command when the cryptographic processing unit receives the incorrectly sequenced command, since Ehrtam states at column 80, lines 3-7 that out of sequence commands or commands executed at the wrong time would cause the destruction or loss of good data in the cryptoprocessors or provide useless data from the cryptoprocessors. Therefore, rejecting incorrectly sequenced commands ensures data integrity.

16. Regarding Claims 3 and 18, Ehrtam teaches the storage device and method wherein when the cryptographic processing unit receives the incorrectly sequenced command, the cryptographic processing unit interrupts the cryptographic input/output processing to which the command belongs (column 36, line 61 to column 37, line 13, column 80, line 3-67).

17. Regarding Claim 4 and 13, Ohta discloses the storage device and method according to claims 1 and 12, wherein the number of the cryptographic input/output processing which can be performed simultaneously by the storage device is predetermined in accordance with a performance of the storage device (column 2 lines 24-61 wherein the processing is achieved by breaking the data into predetermined data blocks according to the data block size for authentication processing).

18. Regarding Claims 5, 8, and 14, Ohta discloses the storage devices and method according to claim 1, 7, and 12 wherein in response to a request from the host device, the storage device provides to the host device the maximum number of cryptographic input/output processing which can be performed simultaneously by the storage device (column 2 lines 2-61 wherein the blocks are accumulated until the appropriate maximum size for the accumulation buffer then outputted).

19. As per claims 10 and 12, Ohta discloses a host device and method which exchanges data with a storage device that is capable of simultaneously performing a plurality of series of cryptographic input/output processes for encrypting data to be secured and inputting/outputting the data, the host device comprising:

a controller which divides the cryptographic input/output processing into a plurality of sequenced subprocesses and issues commands sequentially to the storage device thereby allowing the storage device to execute a subprocess to be executed on the storage device side (column 6 lines 1-20, and description of figure 3 particularly in column 6 lines 39-58); and

a cryptographic processing unit which carries out encryption or decryption that is required of the cryptographic input/output process (column 2 lines 7-11), wherein when the controller issues a command, the controller attaches identifying information to the command to identify to which one of the plurality of cryptographic input/output processes the command belongs (column 6 lines 1-20 where processing information is the identifying information).

20. Ohta does not teach a controller that issues the command via the bus electrically connecting the host device and the storage device deallocates the bus for another command and wherein the cryptographic processing unit manages the sequence of commands executed in each cryptographic input/output processing and rejects the execution of an incorrectly sequenced command when the cryptographic processing unit receives the incorrectly sequenced command.

21. Arimilli teaches a system controller that manages a plurality of electrical devices, wherein a bus is deallocated based on a received command (column 2, line 64 to column 3, line 13).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made for the bus to be deallocated when a command was issued, since Arimilli states at column 3, lines 9-13 that it would support upgrades of coherency state information, thereby providing for a more stable system.

23. Ehram discloses wherein the cryptographic processing unit manages the sequence of commands executed in each cryptographic input/output processing (column 14, lines 6-58, column 53, lines 11-59, column 58, lines 31-67) and issuing a procedural error when an incorrect sequence of commands is received (column 36, line 61 to column 37, line 13, column 80, line 3-67).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to manage the sequence of commands executed in each cryptographic input/output processing and reject the execution of an incorrectly sequenced command when the cryptographic processing unit receives the incorrectly sequenced command, since Ehram states at column 80, lines 3-7 that out of sequence commands or commands executed at the wrong time

would cause the destruction or loss of good data in the cryptoprocessors or provide useless data from the cryptoprocessors. Therefore, rejecting incorrectly sequenced commands ensures data integrity.

25. Regarding Claim 11, Ohta discloses the host device according to claim 10, wherein the controller issues a command to allocate a process system for performing the cryptographic input/output processing prior to initiation of the cryptographic input/output processing (column 6 lines 1-20 where processing information is the identifying information and the determination of which kind of processing the data requires is interpreted to be allocating a process system).

26. Regarding Claim 15, Ohta discloses the data input/output method according to claim 13, further comprising, prior to performing the cryptographic input/output processing, selecting and allocating identifying information for identifying the cryptographic input/output processing to be performed from among the prepared number of pieces of identifying information determined in the determining step (column 6 lines 1-20 where processing information is the identifying information and the determination of which kind of processing the data requires is interpreted to be allocating a process system).

27. Regarding Claim 16, Ohta discloses the data input/output method according to claim 14, further comprising, prior to performing the cryptographic input/output processing, selecting and allocating identifying information for identifying the cryptographic input/output processing to be performed from among the prepared number of pieces of identifying information determined in

the determining step (column 6 lines 1-20 where processing information is the identifying information and the determination of which kind of processing the data requires is interpreted to be allocating a process system).

28. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta in view of Arimilli and Ehram applied above, and further in view U.S. Patent Application Publication No. 2003/0226029 A1 to Porter et al., hereinafter Porter.

29. Regarding claims 6 and 9, Ohta and Ehram do not teach the storage devices, wherein the storage medium comprises a normal data storing unit and a confidential data storing unit, the normal data storing unit storing normal data to be exchanged bypassing the cryptographic processing unit, the confidential data storing unit storing the secret data to be exchanged via the cryptographic processing unit.

30. Porter teaches the storage devices, wherein the storage medium comprises a normal data storing unit and a confidential data storing unit, the normal data storing unit storing normal data to be exchanged bypassing the cryptographic processing unit, the confidential data storing unit storing the secret data to be exchanged via the cryptographic processing unit (Porter paragraph 39 common memory and protected memory).

31. It would be obvious to one of ordinary skill in the art at the time the invention was made to incorporate both a protected and common memory in the cryptographic system of Ohta, since Porter states in paragraph [0039] that a region of memory can be designated as protected from the unauthorized use by using encryption.

Conclusion

32. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

33. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

34. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian LaForgia whose telephone number is (571)272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

35. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christian LaForgia/
Primary Examiner, Art Unit 2439

clf